EXECUTIVE SUMMARY

STACK ETF Concept - Executive Summary

Institutional Editorial Binder

Unified formatting, refined language, headers, footers, page numbering, terminology alignment, and section-to-section continuity.

Prepared for strategic review and implementation discussions

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Section 1

Document Overview

physical infrastructure layer of the AI supercycle: advanced packaging, testing, inspection, metrology, high-purity systems, and semiconductor buildout bottlenecks. The opportunity is to turn an underrepresented AI infrastructure category into a clean, ETF-ready product. Internal discussion material only. Not investment advice, not legal advice, not a prospectus, not a solicitation, and not official ETF performance material. Performance comparisons, if discussed separately, should be described as illustrative current-weighted basket analysis, not live ETF performance.

Section 2

Data Tables

Table 1

Wall Street already has semiconductor ETFs and AI ETFs. What it lacks is a focused ETF built around advanced packaging and the physical infrastructure layer that AI chips depend on.

Product Concept $STACK is a proposed Advanced Packaging & AI Infrastructure ETF concept designed to target the physical bottleneck layer behind AI chip scaling: advanced packaging, assembly, inspection, metrology, testing, burn-in, high-purity systems, and related semiconductor infrastructure. Market Gap Existing semiconductor and AI ETFs tend to focus heavily on broad semiconductor exposure, mega-cap chip designers, or general AI beneficiaries. $STACK is designed to isolate the companies supporting the backend and infrastructure bottlenecks required to physically manufacture, package, test, and scale AI chips.	**Differentiation SMH owns the chip race. $STACK owns the bottleneck. The strategy is built around the idea that AI compute demand creates pressure throughout the physical supply chain - packaging capacity, test capacity, yield control, thermal validation, power, cooling, and high-purity systems. Operator Edge $STACK was built from an infrastructure/operator perspective, not only from a financial screen. The thesis comes from understanding where real buildout constraints appear: facility construction, process flows, tooling demand, labor pipelines, and the physical systems behind AI chip production.**

Table 2

Tier	Allocation	Purpose
Tier 1 - Anchors	30%	Institutional foundation: large, liquid semiconductor equipment and process-control leaders.
Tier 2 - Core Assembly	25%	Advanced packaging, assembly, OSAT, semiconductor test, and backend chip integration.
Tier 3 - Specialized Infrastructure	30%	Inspection, metrology, cleaning, test infrastructure, high-purity systems, and facility-adjacent suppliers.
Tier 4 - High-Risk Speedboats	15%	Capped exposure to smaller, specialized, higher-volatility bottleneck companies.

Table 3

Selection Methodology 1. Liquidity screen: minimum average daily dollar-volume threshold to support ETF scalability and reduce thin-name execution risk. 2. Purity screen: meaningful exposure to semiconductor equipment, advanced packaging, testing, inspection, metrology, high-purity systems, or AI infrastructure. 3. Operator / field-alpha audit: the company must connect to a real physical bottleneck inside modern fabs, packaging operations, testing environments, or hyperscale AI infrastructure buildouts.	**Demand Signal A subscription-style landing page was launched as an early demand test for the $STACK category. Initial traffic after limited Facebook promotion showed early interest. This is not proof of ETF demand, but it is a useful signal that the advanced packaging and AI infrastructure story is understandable outside Wall Street. Tidal Discussion Ask Get Tidal's feedback on active vs. index structure, liquidity and capacity constraints, seed capital, launch economics, compliance path, filing timeline, and whether $STACK should move into formal diligence.**